Remarks

In view of the above amendments and the following remarks, reconsideration of the rejections and further examination are requested.

The Examiner has failed to consider Sarginson and Siong, included with the Information Disclosure Statement filed on September 1, 2005. Enclosed herewith are copies of these references and the form PTO-1449 originally filed on September 1, 2005, along with a date-stamped postcard receipt as evidence of their submission. It is respectfully requested that the Examiner return a completely initialed copy of the form PTO-1449.

Claims 1, 3 and 4 have been rejected under 35 U.S.C. §112, second paragraph, as being indefinite. Specifically, the rejection indicates that the term "instruction" in claims 1, 3 and 4 does not have proper antecedent basis in some instances. Therefore, claims 1, 3 and 4 have been amended so as to address this rejection. As a result, withdrawal of the rejection is respectfully requested.

Claims 1, 3-5, 7 and 8 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Kawakami (US 6,332,058), Siong (US 6,028,632) and Haskell (US 5,159,447). This rejection is respectfully traversed and submitted to be inapplicable to the claims for the following reasons.

Claim 1 is patentable over the combination of Kawakami, Siong and Haskell, since claim 1 recites a multiple decoding apparatus including, in part, a data flow controller for distributing two or more encoded data stored in a buffer for each data type and transferring the two or more encoded data in accordance with provided transfer conditions. The combination of Kawakami, Siong and Haskell fails to disclose or suggest the data flow controller of claim 1.

Kawakami discloses an MPEG server 16 having a core 18 that receives information material (an MPEG stream) 14 and an external controller 24 operable to supply a control signal 26 to the core 18. The MPEG server 16 also includes a number of hard disk drives (HDDs) 20, DMA buffers 30, a time-divisional multiplexing controller 40, gate controllers 32, decoder buffers 34 and decoders 22. (See column 4, line 47 – column 5, line 54 and Figures 1 and 2).

In a recordation operation, the MPEG server 16 receives the control signal 26 indicating that the MPEG server 16 is to record the information material 14. The MPEG server 16 then divides the

information material 14 into a number of cells CE each having a size of four bytes. The cells CE are recorded on the HDDs 20 such that the first cell is stored on HDD 20-1, the second cell is stored on HDD 20-2, the third cell is stored on HDD 20-3, etc. Therefore, it is apparent that the information material 14 is split into a number of cells CE and the HDDs 20 are used to store the cells CE in parallel. (See column 5, line 10 – column 6, line 7).

In a reproduction operation, the MPEG server 16 receives a control signal 38 from a CPU group 36 indicating that the MPEG server 16 is to reproduce the information material 14. The cells CE are read from the HDDs 20 and stored in DMA buffers 30 which respectively correspond to the HDDs 20. The cells CE are written to the DMA buffers 30 in clusters CT, which are larger than the cells CE. The controller 40 then controls the output of the information stored in the DMA buffers 30 such that desired information from each of the DMA buffers 30 is read at a desired time point. The gate controllers 32 operate so as to allow the information output by the DMA buffers 30 under the control of the controller 40 to only be supplied to the appropriate decoder buffer 34. (See column 5, lines 34-37; column 6, lines 46-49; column 7, lines 11-16 and 55-58; and Figures 1 and 2).

Once the information material 14 is properly stored in the decoder buffer 34, it is read out from the corresponding decoder 22 as packets PT and decoded into a video signal VS and an audio signal AS to reproduce the information material 14. (See column 6, lines 42-59 and Figure 2).

Claim 1 of the present invention recites that the data flow controller is for distributing two or more encoded data stored in a buffer for each data type and transferring the two or more encoded data in accordance with provided transfer conditions. From this recitation of claim 1, it is apparent that the data flow controller distributes encoded data based on data type. It is submitted that Kawakami fails to disclose or suggest such a feature.

Based on the above discussion of Kawakami, the information material 14 is split into the cells CE in 4-byte groups and stored on the HDDs 20 such that the first cell CE is stored on the HDD 20-1, the second cell CE is stored on the HDD 20-2, the third cell CE is stored on the HDD 20-3, the fourth cell CE is stored on the HDD 20-4, the fifth cell CE is stored on the HDD 20-5, the sixth cell CE is stored on the HDD 20-1, and so on until all of the information material 14 has been stored. Then, during reproduction, the cells CE are read from the HDDs 20 as the clusters CT and stored in the respective DMA buffers 30. Therefore, Kawakami distributes the data to the HDDs 20 and the

DMA buffers 30 based solely on a number of bytes defined for the cells CE and the clusters CT and not on data type.

Also, in the rejection, it is indicated that the controller 40 corresponds to the claimed data flow controller. However, the controller 40 controls the output of data from the DMA buffers 30 to one of the decoder buffers 34 so that the information material 14 can be properly decoded by the decoder 22 corresponding to the decoder buffer 34. Kawakami does not disclose or suggest that the controller 40 distributes the data from the DMA buffers 30 to a number of the decoders 22 based on data type. This can be clearly seen from Figure 2, which shows each of the decoders 22 outputing both the video signal VS and the audio signal AS. Further, it is apparent that the MPEG server 16 has the plurality of buffers 34 and corresponding decoders 22 so as to reproduce a number of information materials 14 on many channels (i.e., to increase capacity) and there is no indication of distribution to the decoders 22 based on data type. (See column 5, lines 55-65).

Further, it is noted that, in section 5 of the Office Action, the Examiner indicates that "the MPEG stream of data as shown in Kawakami is based according to a specific type of video, which includes inherent and specific header data...." The Examiner also states in the comments that "the audio AS and the video VS provided by the information materials 14 in the MPEG stream of Kawakami ... are equivalent to the "data type" as claimed, and the controller 40 of Kawakami corresponds to the data flow controller ...." Regarding these comments, it is noted that the MPEG stream of the information material 14 supplied to the MPEG server 16 can be classified as a data type. However, the MPEG stream is always treated in the same manner by the MPEG server 16. That is, the MPEG stream is split into the cells CE and stored on the HDDs 20. The cells CE are then read from the HDDs 20 and stored in DMA buffers 30 in clusters CT, which are larger than the cells CE. The controller 40 then controls the output of the information stored in the DMA buffers 30 such that desired information from each of the DMA buffers 30 is read at a desired time point. Based on the discussion of the operation of the MPEG server 16, it is clear that there is no distribution performed by the controller 40, or any other portion of the MPEG server 16 for that matter, that are based on data type. Therefore, that the MPEG stream constitutes a "data type" does not mean that the MPEG server 16 performs distribution based on data type. As a result, it is believed apparent that Kawakami fails to disclose or suggest the data flow controller as recited in

claim 1.

Therefore, in order for the combination of Kawakami, Siong and Haskell to render claim 1 obvious, at least one of Siong and Haskell must disclose or suggest the data flow controller recited in claim 1. However, Siong is relied upon as disclosing a separate buffer manager for controlling the outputs of a plurality of separate buffers and Haskell is relied upon as disclosing a buffer controller for a variable bit rate channel. Neither of these references discloses or suggests the data flow controller of claim 1. As a result, the combination of Kawakami, Siong and Haskell fails to render claim 1 obvious.

As for claim 5, it is patentable over the combination of Kawakami, Siong and Haskell for reasons similar to those discussed above in support of claim 1. That is, claim 5 recites, in part, distributing two or more encoded data stored in a buffer for each data type and respectively storing the two or more encoded data in the plurality of separate buffers, which feature is not disclosed or suggested by the references.

Because of the above-mentioned distinctions, it is believed clear that claims 1, 3-5, 7 and 8 are allowable over the references relied upon in the rejection. Furthermore, it is submitted that the distinctions are such that a person having ordinary skill in the art at the time of invention would not have been motivated to make any combination of the references of record in such a manner as to result in, or otherwise render obvious, the present invention as recited in claims 1, 3-5, 7 and 8. Therefore, it is submitted that claims 1, 3-5, 7 and 8 are clearly allowable over the prior art of record.

In view of the above amendments and remarks, it is submitted that the present application is now in condition for allowance. The Examiner is invited to contact the undersigned by telephone if it is felt that there are issues remaining which must be resolved before allowance of the application.

Respectfully submitted,

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